ABSTRACT

A serial access memory low in current consumption, capable of restraining an increase in chip size even if memory capacity increases. The serial access memory has a first and a second memory arrays each having memory cells electrically connected to corresponding bit lines, signal lines provided in common between the memory arrays and electrically connected to the corresponding bit lines through first transfer circuits, write registers electrically connected to the corresponding signal lines through a second transfer circuit, a write bus electrically connected to the write registers through a third transfer circuit, an input circuit electrically connected to the write bus, read registers electrically connected to the corresponding signal lines through a fourth transfer circuit, a read bus electrically connected to the read registers through a fifth transfer circuit, and an input circuit electrically connected to the read bus.